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Design of Four Bit FLASH ADC using Clocked Digital Comparator

Abhishek madankar, Prachi Palsodkar

Dept of Electronics Engg.
YCCE College of Engineering
Nagpur, Maharashtra India

***Abstract*— This thesis describes the design of high speed FLASH ADC using clocked digital comparator with 4-bit resolution.The comparator is designed in a 180nm CMOS technology with supply voltage of 1.8 V.**
High speed clocked digital comparator with inverter configuration is used for dynamic offset suppression. As a result, a significant improvement of speed and reduction of area and power consumption is achieved.
Thesis describe the design of 4-bit Flash ADC using Multiplexer based decoder and clocking circuit.
The simulation results are derived using Cadence environment. It fulfills all the Performance requirements.

***Keywords*—** mux, cmos-cdc, adc, tiq

I. INTRODUCTION

The full-flash type A/D converter architecture is the most attractive solution for high speed A/D converter design, the speed and resolution is inversely related to each other hence for high speed application the resolution must kept small as possible. The comparator structure is most critical part of flash A/D.

Some of the problems of the conventional comparator structures used in A/D designs can be
listed as follows [1]:

1. large transistor area for higher accuracy
2. DC bias requirement
3. charge injection errors
4. metastability errors
5. high power consumption
6. Resistor or capacitor array requirement.

The clocked digital comparator is made up of two stages, the first stage is transistor inverter quantizer and second stage is transmission gate. The first stage provides the internal reference voltage for comparison, internal reference voltage is generated by varying the transistor size due to which resistor ladder network will not required for generation of internal reference voltage and second stage provide the switching instance (sampling period).

II. CDC STRUCTURE

The cdc consist of two cascaded cmos inverter followed by transmission gate as shown in fig (1).

The analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) by means of transistor sizing [5]. Since the transistor channel length, L, is more effective than the channel width, W, in controlling the performance (fT a 1/L2), L is kept constant and only W is changed during the design process.

The second inverter stage is used for increased gain and logic level inversion so that the circuit behaves as an internally set comparator circuit. The key point with the second stage is that the second stage must be exactly the same as the first stage to maintain the same DC threshold levels, and to keep the linearity in balance for the voltage rising and falling intervals of high frequency input signals.

It can be shown that the Vm point on the VTC of a CMOS inverter, which is shown in Fig. 1(a), can approximately be given by the following equation

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{dd} - \left|V_{Tp}\right|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

where Vtn and Vtp are the threshold voltages for NMOS and PMOS devices, respectively; and Kn = (W/L)n . mn Cox Kp = (W/L)p . mp Cox.

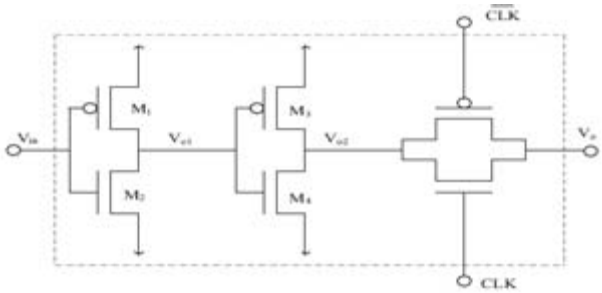


Figure 1: Clocked Digital Comparator

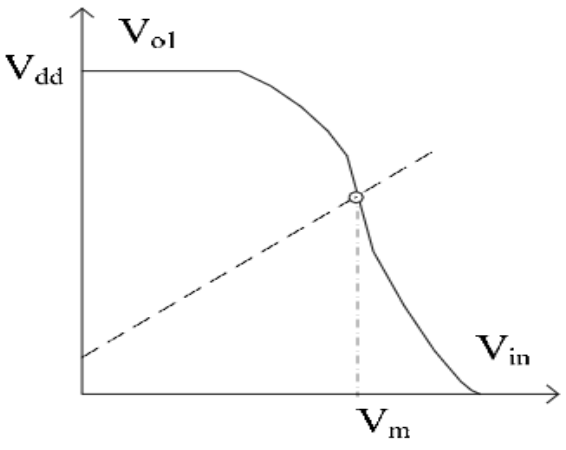


Figure 1(a): VTC for inverter

III. THERMOMETER TO BINARY CONVERTER

A multiplexer (mux) based 4-bit version of thermometer code to binary code converter is as shown in Fig. 2. This circuit is based on 2:1 multiplexers connected as a tree. Each level of the tree divides the input thermometer scale in two and calculates one of the bits in the binary output. For N-bit flash ADC the most significant bit (MSB) of the binary output is high if more than half of the outputs in the thermometer scale are logic '1'. Hence MSB is the same as the thermometer output at level 2N-1. To find the value at the second most significant bit (MSB-1) the original thermometer scale is divided into two partial thermometer scales, separated by the output level at 2N-1. The partial thermometer scale is chosen by a set of 2:1 multiplexers where the previous binary output is connected to the control input of the multiplexers. MSB-1 is then found from the chosen partial thermometer scale in the same way as MSB was found from the full thermometer scale. The lower partial thermometer scale is used if the output at level 2N-1 is logic '0' otherwise the upper partial thermometer scale is used. This is continued recursively until only one 2:1 multiplexer remains. Its output is the least significant bit of the binary output [8]. In this approach 2:1 mux is designed using CMOS transmission gate and an inverter.

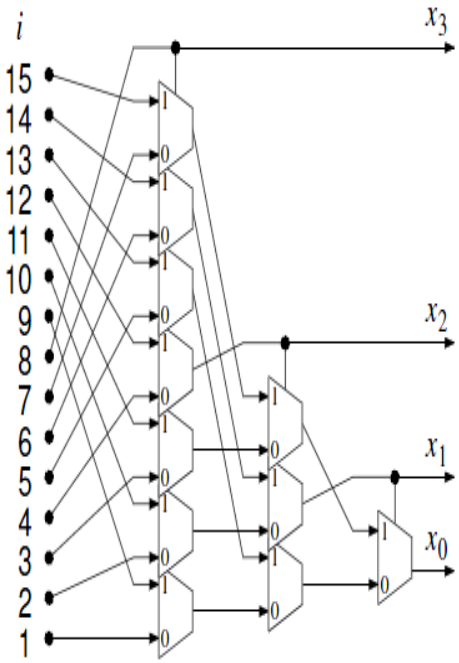


Figure 2: Multiplexer based decoder for N=4 bits

IV. EXPERIMENTAL RESULT

The proposed Quantized comparator has been designed for TSMC 0.18u technology.

The VTC of a set of clocked digital comparator is shown in figure 3, clearly depicting the desired step changes in the switching voltage of the comparator. The figure 4 shows the output of 4 bit ADC using CDC. The table (1) shows the calculation of differential non linearity error.

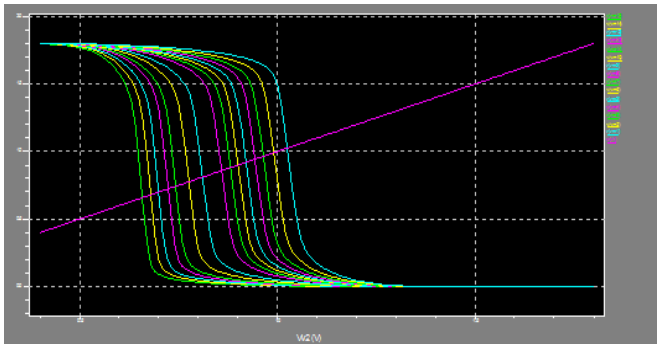


Figure 3: VTC for fifteen CDC comparator

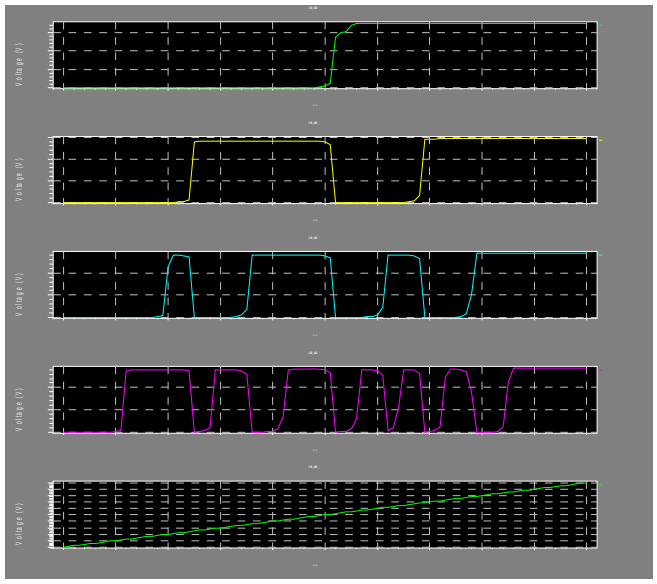
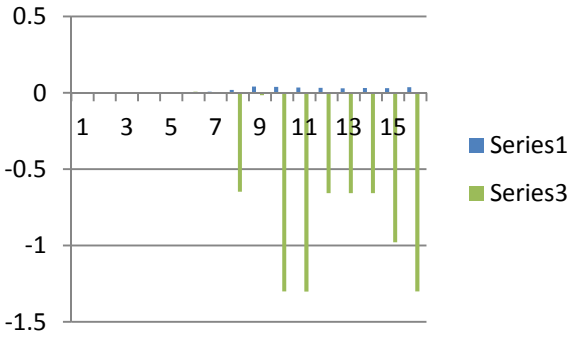


Figure 4: Simulation result for 4 bit flash ADC using CDC

Table (1): shows the calculation of differential non linearity (DNL) and Integral non linearity error

Sr No	Actual Value (LSB)	Ideal Value (1LSB=.1125)	DNL=Actual Value-Ideal Value	INL
1	0.65	0.653	0	0
2	0.68	0.676	0.00444	-0.0047
3	0.69	0.700	-0.00212	0.002356
4	0.72	0.723	0.00032	0
5	0.74	0.747	-0.00324	0.007
6	0.77	0.770	0.0072	0.002356
7	0.81	0.794	0.01864	-0.648
8	0.85	0.817	0.04108	-0.016
9	0.88	0.841	0.03852	-1.3
10	0.9	0.865	0.03496	-1.301
11	0.92	0.888	0.0324	-0.657
12	0.94	0.912	0.02984	-0.657
13	0.96	0.935	0.03128	-0.657
14	0.99	0.959	0.03072	-0.979
15	1.02	0.982	0.03716	-1.3



V. CONCLUSION

CDC Comparator Flash ADC have been designed and simulated with 180 nm technology.

The result obtained are indicating that the DNL is reduced which will affect the speed of ADC.

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